Remarks

Claims 1-2 are pending in the application. Claims 1-2 are rejected. Claim 2 is objected to. Claim 2 is amended. The Abstract is objected to. All rejections and objections are respectfully traversed.

Claim 2 is objected to based on a typographical error, which is corrected by amendment herein.

The Abstract of the Disclosure is objected to. A substitute Abstract of the Disclosure, which will replace any previous version of the Abstract of the Disclosure, is submitted herewith as "Appendix A."

Claims 1 and 2 are rejected on the grounds of non-statutory obviousness-type double patenting as being unpatentable over claims 1 and 30 of U.S. Patent 6,618,395 in view of Buchanan et al., (U.S. 6,970,435 – Buchanan).

The double patenting rejection above is traversed below in the arguments asserted with respect to the 35 U.S.C 102(e) rejection based on Buchanan, as both rejections present the same erroneous arguments direct to the same elements of what is claimed, based on the teaching of Buchanan.

Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Buchanan.

To get straight to the point, the Examiner erroneously references a section of Buchanan that teaches serializing (by multiplexing) lesser width parallel data

words for transmission, to teach generating lesser width parallel data words, as claimed. More particularly, claim 1 recites that the lesser width parallel data words are concurrently generated such that "all adjacent bits of said greater width parallel data word are contained in different ones of said lesser width parallel data words." The Examiner parses the recited 'concurrently generating' step by referring to two different sections of Buchanan. The first section describes a generating step based on partitioning the greater width parallel data word. The second section refers to a serialization step of already generated parallel data words (nibbles), which is useless for teaching the generation step, as claimed.

First, col. 4, lines 54-56 and 62 -64 is referenced to teach the partial element of 'concurrently generating a plurality of lesser width parallel data words containing parallel data from a greater width parallel data word' as claimed. There is no teaching that the generating of lesser width parallel data words is done concurrently, as claimed. However, the Applicant does not dispute that generating a plurality of lesser width parallel data words containing parallel data from a greater width parallel data word is known, see, e.g., col. 4, lines 54-64, below:

serial link. In one embodiment of the present invention, 16-bit parallel data streams are supplied to DASL interface.
55 The bit streams are partitioned into four groups of four bit (4 bits=1 nibble) streams. Each of the nibbles is processed according to the teaching of the present invention and is sent over a serial link. As a consequence, to transmit the 16-bit, four serial links would be required. Each nibble of data is
60 processed in the same way; therefore, the description of one (set forth hereinafter) is intended to cover the processing of the others. The four parallel data bit streams are transformed into a high speed serial bit stream by latching each of the four bit streams in one of the Latch L1 through L4 and

The Examiner correctly indicates, by parsing the claim element rejection with different referenced sections, that the above section fails to teach concurrently generating ...'such that all adjacent bits of said greater width

parallel data word are contained in different ones of said lesser width parallel data words' as claimed. This is a key aspect of the invention. Partitioning does not teach the limitation. To teach this, the Examiner points to col. 5, lines 18-21 and 60 – 64. However, the referenced section teaches *serializing* lesser width parallel data words (nibbles) already generated by partitioning step taught in line 55 of col. 4, see above. Both sections of col. 5 referenced by the Examiner explicitly refer to serializing already generated nibbles, see col. 5, lines 14-21, below:

> FIG. 2A shows another embodiment of the transmitter circuit. As stated previously, the function of the transmitter circuit is to serialize nibbles of data onto separate serial streams that are transmitted on separate serial links. The nibble of data is selected from parallel bit streams. Four latches labelled 10, 11, 12 and 13 receive data labelled DATAIN0, DATAIN1, DATAIN2 and DATAIN3. The data are from parallel bit streams. Each of the latches comprises

A person of ordinary skill in the art would readily understand that the above teaches serialization of already generated nibbles and would never be confused with a step of concurrently generating lesser width parallel data words as claimed. It should be understood that by the teaching of Buchanan, adjacent bits of a lesser width parallel data word would interleaved with bits of other lesser width parallel data words, but the lesser width words have already been generated. Buchanan serializes nibbles generated by partitioning, as the invention does in the next element, "serializing said scrambled data words," by serializing concurrently generated parallel data words having the distinction that "all adjacent bits of said greater width parallel data word are contained in different ones of said lesser width parallel data words."

6

The same is true for the Examiner's reference to col. 5, lines 60-64. The
section inclusive of the Examiner's referenced lines refers to the timing
diagram for the serialization process, see col. 5, lines 56-64, below:

> FIG. 2B shows a timing diagram for the circuit in FIG.
> 2A. The first graph in the figure labelled OSC 125 represents
> the basic clock. The graph labelled Output 125 Latches
> shows the information which is outputted from latches L0
> through L3. The number 3210 represents the order in which   60
> the bits are outputted from the latches. As can be seen from
> FIG. 2A, the bits are labeled DATAIN0, DATAIN1,
> DATAIN2 and DATAIN3. The output is in the order, 3-2-
> 1-0. The graph labelled Output 125 MUXes represents the

A person of ordinary skill in the art would readily understand that the above
section provides detail for the multiplexing (serializing) of the already
generated lesser width parallel data words (nibbles). Multiplexing parallel
data words can never teach generating parallel data words.

An important distinction between Buchanan and the invention is that
Buchanan teaches generating nibbles by "partitioning." There is absolutely
no description of lesser width parallel data words concurrently generated
from a greater width parallel data word such that "all adjacent bits of said
greater width parallel data word are contained in different ones of said lesser
width parallel data words," as claimed. The next step recited in the invention
serializes these lesser width parallel data words. Buchanan can never
anticipate what is claimed at least because he fails to teach concurrently
generating lesser width parallel data words from a greater width parallel data
word in the manner recited in claim 1. The Examiner erroneously refers to a
parallel data word serializing step to teach a parallel data word generation
step. Therefore, the Examiner is requested to reconsider and withdraw the
rejections based on Buchanan.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Buchanan in view of Nishida, et al., (U.S. 5,978,486 – "Nishida").

As stated above with respect to claim 1, Buchanan fails to teach lesser width parallel data words generated from a greater width parallel data word such that "all adjacent bits of said greater width parallel data word are contained in different ones of said lesser width parallel data words," as claimed. The Examiner erroneously combined partitioning to generate the words and serializing the generated words to transmit them, which can never teach what is claimed.

Nishida is referenced to teach scrambling the data in the lesser width parallel data words. Nishida teaches a scrambling parallel data, see e.g. col. 18, lines 33-39, below:

> A fourth embodiment of the present invention relates to a
> data scrambling apparatus that receives information data to
> 35 be scrambled, by 8 bits in parallel and outputs scrambled
> data by 8 bits in parallel. FIG. 7 shows an example of the
> data scrambling apparatus. In order to facilitate and embody
> the explanation, a generating polynomial, $G(X)=1+X^7+X^9$, is employed.

Scrambling data, including parallel data, is known. What Nishida, alone or in combination with Buchanan, fails to make obvious is scrambling lesser width parallel data words concurrently generated form a greater width parallel data word such that 'all adjacent bits of said greater width parallel data word are contained in different ones of said lesser width parallel data words,' as claimed. At best, the proposed combination might teach scrambling *partitioned* parallel data words, but can never teach or suggest such that 'all adjacent bits of said greater width parallel data word are contained in different ones of said lesser width parallel data words,' as claimed.
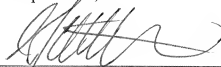
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Further, there is no motivation to combine Buchanan with Nishida in either reference. The Examiner's alleged motivation to combine the references, and his supportive reference to Buchanan at col. 1, lines 26-29, is non-sequitor.

It is believed that this application is now in condition for allowance. A notice to this effect is respectfully requested. Should further questions arise concerning this application, the Examiner is invited to call Applicant's attorney at the number listed below.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 50-3650.

Respectfully submitted,
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9